REMARKS

Claims 1-43 were pending in the application. Claims 6, 34 and 43 are canceled. Claims 44-45 are newly added. Support for new Claims 44-45 is in the Applicants specification as originally filed. (*See* page 14, line 11 – Page 15, line 3.)

Claims have been deemed rejected under 35 U.S.C. § 103(a) and 35 U.S.C. § 102(e). Of the claims, Claims 1, 26, 27, 41 and 43 are independent claims. The specification has been amended to correct typographical errors. The claims as now amended are believed to be patentable over the cited references.

Regarding Rejections under 35 U.S.C. § 112

Claim 43 has been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 43 has been rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

As claim 43 has been canceled, this rejection is moot.

Regarding Rejections under 35 U.S.C. § 102(e)

Claim 26 has been rejected under 35 U.S.C. § 102(e) as being deemed anticipated by Ishigure (JP 3-17891). Claim 43 has been rejected under 35 U.S.C. § 102(e) as being deemed anticipated by Amdahl (U.S. Patent Number 6,005,428.)

Cited prior art, Ishigure is directed to a dynamic refresh system in which refresh time is reduced by switching a refresh clock to a different frequency with a selector. As shown in Fig. 1, a selector 10 selects a clock from clock oscillator 7 or clock oscillator 8 dependent on the state of the mode selector 13.

Ishigure does not teach or suggest at least the Applicants' claimed "first port for receiving a first clock signal, the first clock signal being propagated in a forward processing direction in the pipelined processor; a second port for receiving a second other clock signal, the second other clock signal propagated in a reverse processing path in the pipeline processor" as claimed by the

Applicants in amended Claim 26. In contrast, Ishigure merely discusses selecting a source for a clock in a single direction, that is, to the refresh controller. (*See* Ishigure Fig. 1, 4.)

As claim 43 has been canceled, the rejection of Claim 43 is moot. Accordingly, the present invention as now claimed is not believed to be anticipated by or made obvious from the cited art or any of the prior art. Removal of the rejection under 35 U.S.C. 102(e) and acceptance of Claim 43 is respectfully requested.

Regarding Rejections under 35 U.S.C. 103(a)

Claims 1, 27 and 28 are rejected under 35 U.S.C. § 103(a) as being deemed non-obvious over Nakakura (U.S. Patent Number 5,572,714) in view of Janssens et al. (U.S. Patent Number 6,122,751.) Claims 2-11, and 29-42 are rejected under 35 U.S.C. § 103(a) as being deemed non-obvious over Nakakura (U.S. Patent Number 5,572,714) in view of Janssens as applied to Claims 1, 27 and 28, and further in view of Molnar et al. (U.S. Patent No. 5,572,714). Claims 12-25 are rejected under 35 U.S.C § 103(a) as being unpatentable over Nakakura, Janssens and Molnar as applied to Claims 2-11 and 29-42, and further in view of Choe et al. (U.S. Patent No. 6,484,193).

Before discussing the cited references however, a brief review of the Applicants' disclosure may be helpful.

The Applicants claim a pipeline processor having a plurality of processing stages. Along the forward processing path more than one full clock cycle elapses between gating a block of data into a processor element and gating the processed block of data from that processor element into a next processor element. The processing in one stage of the pipeline does not have to be completed before the next data is clocked in. Thus, a given set of data spends a total time within the pipeline stage greater than the duration of one clock cycle which extends the amount of time available for processing in a forward direction. Along the return processing path less than one full clock cycle elapses between gating a block of data into a processor element and gating the processed block of data into a next processor element (previous in the forward path). (*See* Applicants' Specification Page 14, line 11 – Page 15, line 3.) Thus the overall processing time (both forward and reverse directions) is reduced. The bi-directional pipeline that includes a clock distribution circuit. (see page 13, line 12 – line 28, and page 13, line 30 – page 14, line; and Fig. 4.)

Turning to the cited art, Janssens is directed to a pipelined data processing circuit that forms a single stage of a pipeline. The circuit latches data at intermediate phases of a single clock cycle while the data is kept in an initial register to reduce the number of glitches as the data propagates from the initial register to the initial register in the next stage. Data remains in the pipeline stage for one period of the clock. (*See* Abstract.)

Cited prior art, Nakakura is directed reducing the clock cycle in a system for performing pipeline processing. The clock cycle is shorter than the processing time of the slowest logic element by providing latches with different latch timings for delivering data to logic elements. As shown in Fig. 3A, the logic element receives a clock signal 100 at the input of a clock generator 108 and outputs a clock signal ph1. This clock signal ph1 is delayed through a delay element 109 to provide a delayed clock signal ph1. As logic element 107 has a shorter processing time than logic element 106, the clock of latch 2 is delayed by delay 109 allowing the first logic element 106 to have more processing time.

Cited prior art, Molnar discusses a bi-directional pipeline that can control data flow in both directions and allows counter flowing data elements to interact reliably at each stage of the pipeline.

Cited prior art Choe is directed to a pipelined parallel multiplier with a fast clock cycle.

To establish a prima facie case for obviousness under 35 U.S.C. § 103 (a), (1) there must be some suggestion or motivation to combine reference teachings. (2) There must be a reasonable expectation of success. (3) The references when combined must teach or suggest all the claim limitations. For the reasons discussed below, it is respectfully submitted that the Office has not established a prima facie case under 35 U.S.C. § 103(a) for claims 1-25 and 27-42, and that therefore, claims 1-25 and 27-42 are allowable.

Cited prior art Nakakura does not teach or suggest at least the Applicants' claimed "processing element having a forward processing path and a reverse processing path", In contrast, only one path (forward processing path is shown from "data 1" to "data 6". (*See* Fig. 3A.) Furthermore, Nakakura does not teach or suggest the Applicants' claimed "clock distribution circuit in electrical communication with each processing element, a clock signal propagated along the clock distribution circuit arrives at each processing element delayed relative to the clock signal arriving at a preceding processing element" as claimed by the

Applicants in claim 1. In contrast, Nakakura only discusses delaying the clock once to a next stage when the processing time in a previous stage is long compared to the processing time in a next stage to allow the current stage to extend processing time into the unused processing time of the next stage. The next stage provides the additional processing time to the current stage because the current stage delays forwarding the data to the next stage. (*See* Col. 5, lines 46-67; and Fig. 5, stage 2, stage 3.)

Cited prior art Janssens merely discusses a pipelined circuit in which all processing occurs in a single clock cycle. Data is stored in registers in the pipelined circuit at intermediate phases of the single clock cycle. Janssens' discussion of processing in a pipelined circuit during a single clock cycle does not teach or suggest the Applicants' claimed "data processed by a processing element in the forward processing path being gated into an adjacent processing element by the delayed clock signal received by the adjacent processing element at least one clock cycle after data is gated into the processing element". Janssens merely discusses a single stage in which data is gated into the stage (pipeline circuit) at the beginning of a clock cycle and data is gated to the next stage at the beginning of the next clock cycle.

Nakakura's mere discussion of delaying forwarding data to a next pipeline stage when the stages have different processing times in order to give additional processing time to a stage having a long processing time and Janssens' discussion of processing within a single clock cycle does not teach or suggest at least the Applicants' claimed "each processing element having a forward processing path and a reverse processing path". In contrast, Janssens only shows one processing path in a forward direction from initial circuit 8 to final circuit 9. (*See* Fig. 1.)

Thus, Nakakura or Janssens singly or in combination do not teach or suggest at least the applicants' claimed "each processing element having a forward processing path and a reverse processing path" as claimed by the Applicants in claim 1.

Claims 2-25 are dependent on Claim 1 and thus include this limitation over the prior art.

Independent Claim 27 recites a like distinction in terms of a method and thus similarly patentably distinguishes over the prior art. Claims 28-40 are dependent on Claim 27 and thus include this limitation over the prior art.

Furthermore the dependent claims contain even further distinguishing limitations. For example, claim 2 recites "the reverse processing path in each processing element has a process

time shorter than the process time of the forward processing path". Cited prior art, Molnar does not teach or suggest the Applicants' claimed "reverse processing path in each processing element has a process time shorter than the process time of the forward processing path" as claimed by the Applicants in Claim 2 as amended.

Both Nakakura and Janssens are directed to single-direction pipelines and there is no suggestion in Nakakura or Janssens of the need for a bi-directional pipeline. Even if Nakakura and Janssens were combined with the bi-directional pipeline of Molnar the applicant's claimed invention would not result. In fact, the reverse direction in Nakakura would not work because if the data from stage 2 is received earlier from stage 3, stage 2 would not have sufficient time to process the data. In the applicants' claimed invention, the reverse processing path is known to be shorter than the forward processing path and thus the reduced cycle time is sufficient to perform the reverse path processing in each stage of the pipeline. With the design of Nakakura, the reverse direction would not work, because the data from the stage with the delay in the forward direction would not have sufficient time to process the data based on the clock rising edges.

The combination of Choe and the other prior art does not teach or suggest the applicants' claimed invention. In particular, Janssens does not teach or suggest the same delay per stage because Janssens' discussion is limited to a single pipeline stage and Nakakura is directed to a pipeline with stages having a different delay per stage.

Regarding Office Notice

The Examiner has taken Official Notice of the use of the claimed technique of the use of gating to cause equivalent delays was well-known in the art. The Applicants respectfully traverse the Examiner's assertion of Official Notice. The cited prior art does not suggest at least the Applicants' claimed "the clock signal is gated from a preceding processing element to a next processing element, each processing element having therein circuitry for causing a known delay in the clock signal".

Accordingly, the present invention as now claimed is not believed to be anticipated by or made obvious from the cited art or any of the prior art. Removal of the rejections under 35 U.S.C. 102(e) and 35 U.S.C. 103(c) acceptance of Claims 1-5, 7-33, 35-42 and 44-45 is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Concord, MA 01742-9133
Dated: 2/11/05

Amendments to the Drawings

Support for the corrections is in the Applicant's specification as originally filed. Proposed corrections to Figures 1, 2, 6, 7, and 8A-B have been corrected to include labels referred to in the specification. Support for the correction to Figure 1 is provided at Page 10, lines 15-27. Support for the correction to Figure 2 is provided at Page 10, lines 29-31. Support for the correction to Figure 6 is provided at Page 16, line 16-30. Support for the correction to Figure 7 is provided at Page 17, lines 1-16. Support for the correction to Figures 8A-B is provided at Page 18, line 29 – Page 19, line 6.

No new matter is introduced by these corrections. Acceptance of the enclosed amended replacement drawings is respectfully requested.

Attachment: Replacement Sheets
Annotated Marked-Up Drawings

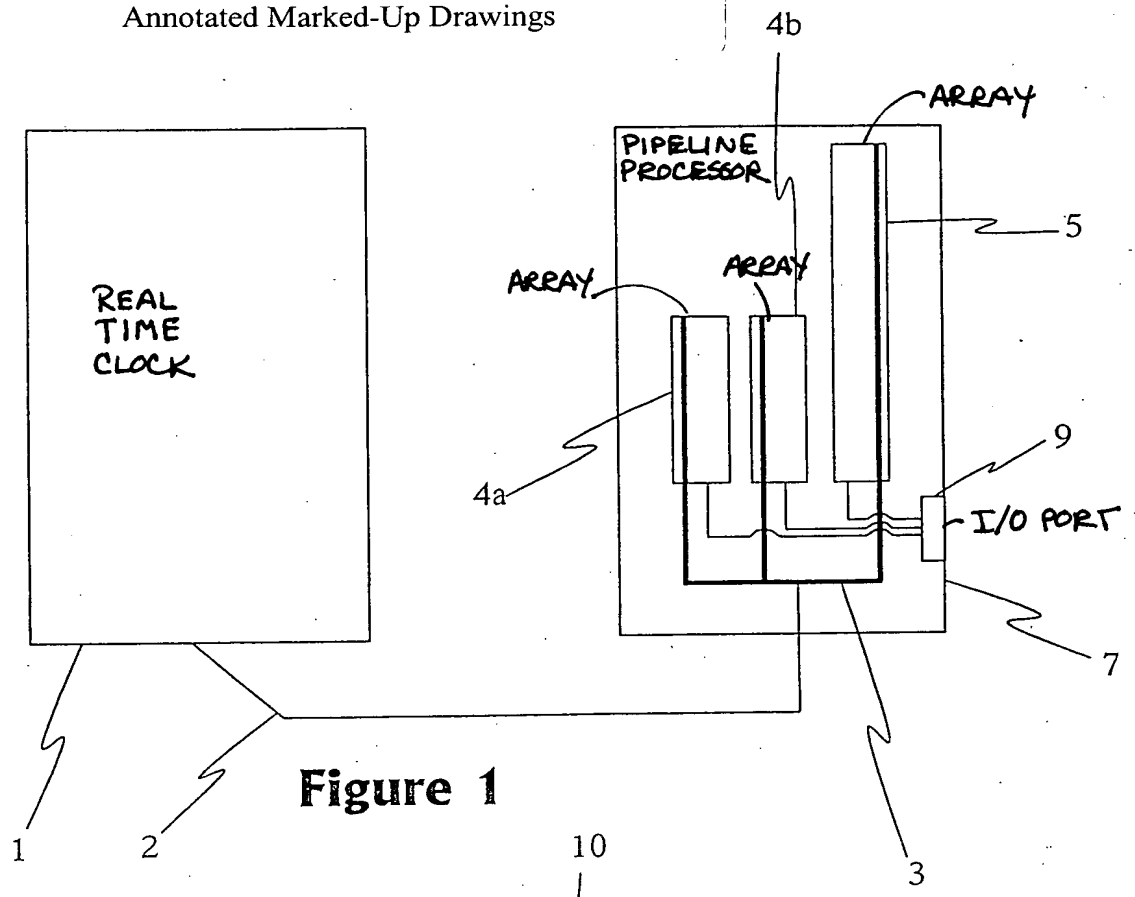


Figure 1

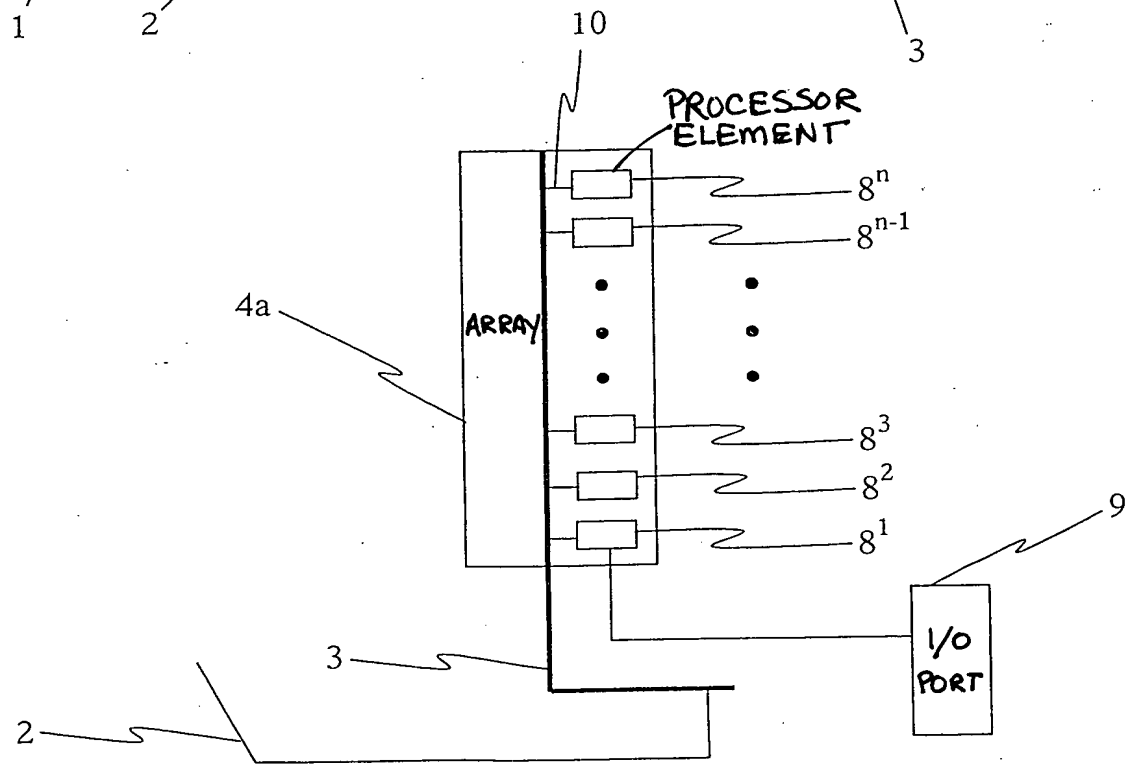
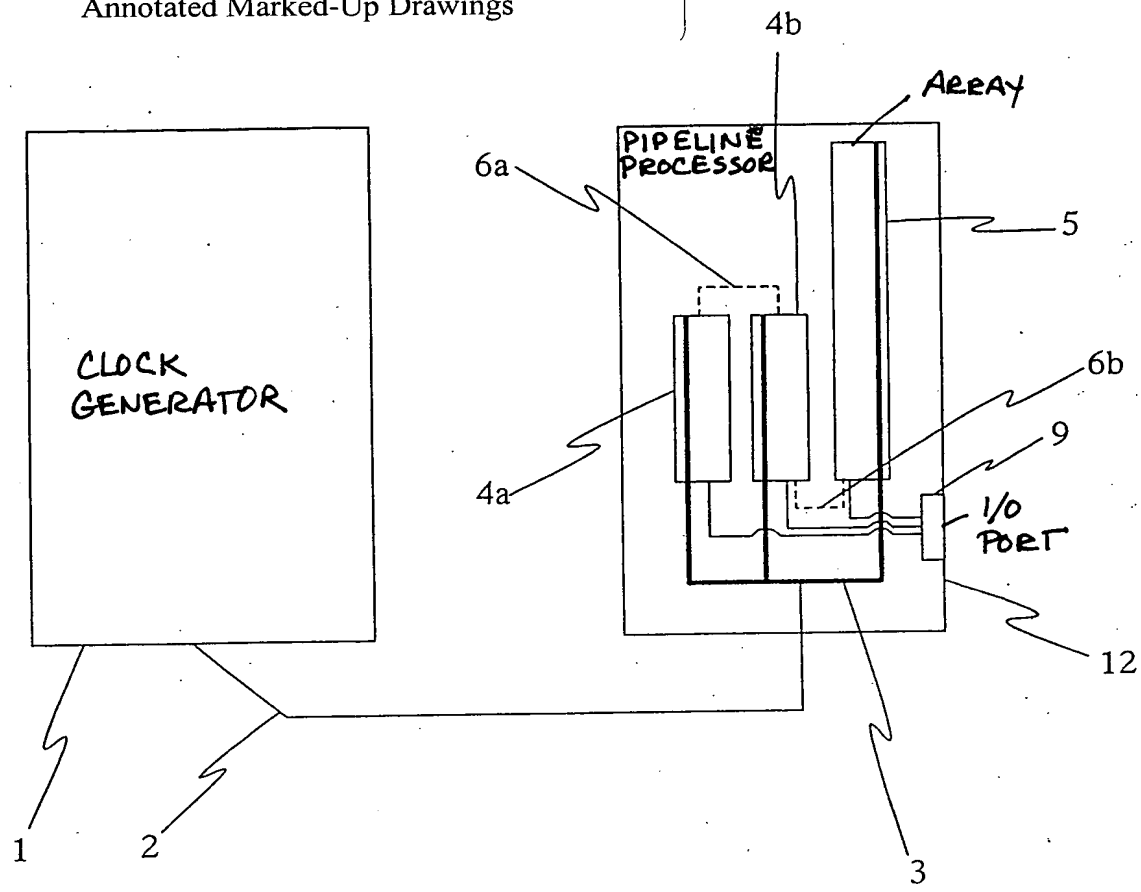


Figure 2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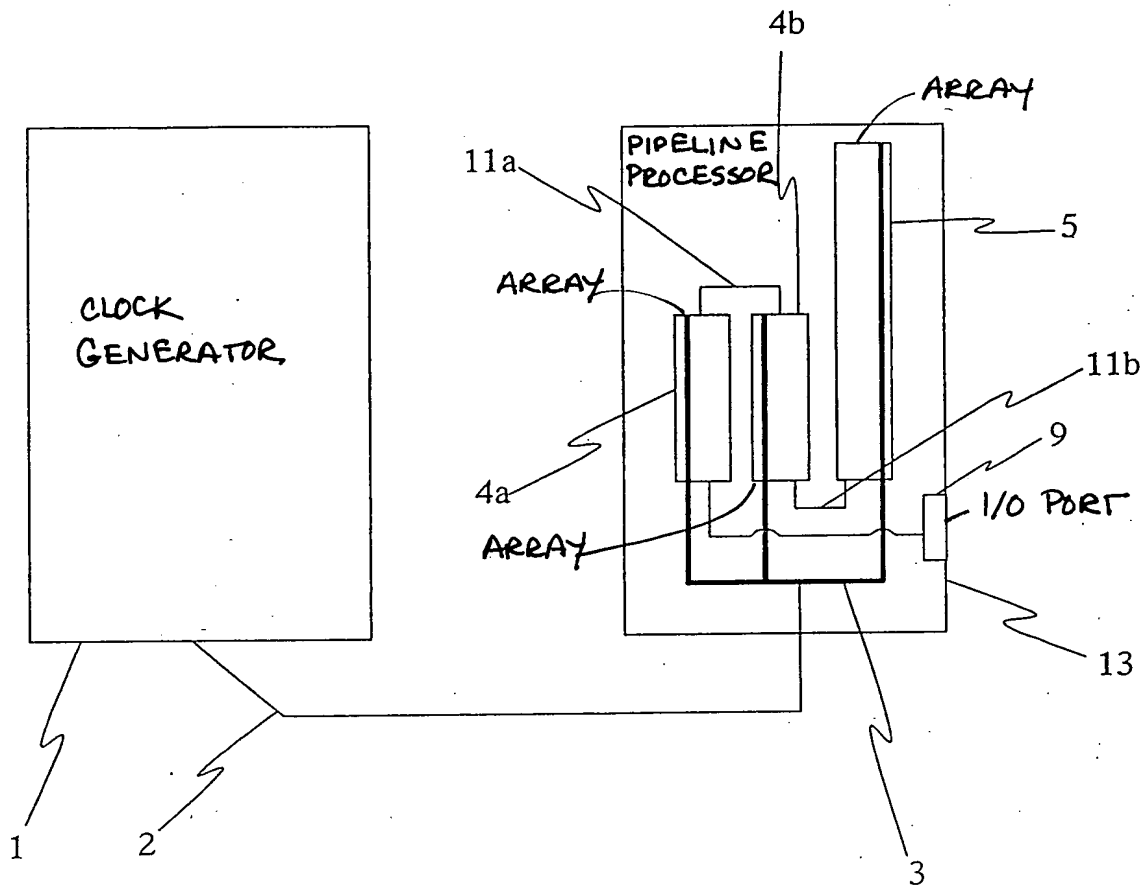
6a
5
CLOCK GENERATOR
6b
9
4a
I/O PORT
12
1
2
3

Figure 6


4b
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PIPELINE PROCESSOR
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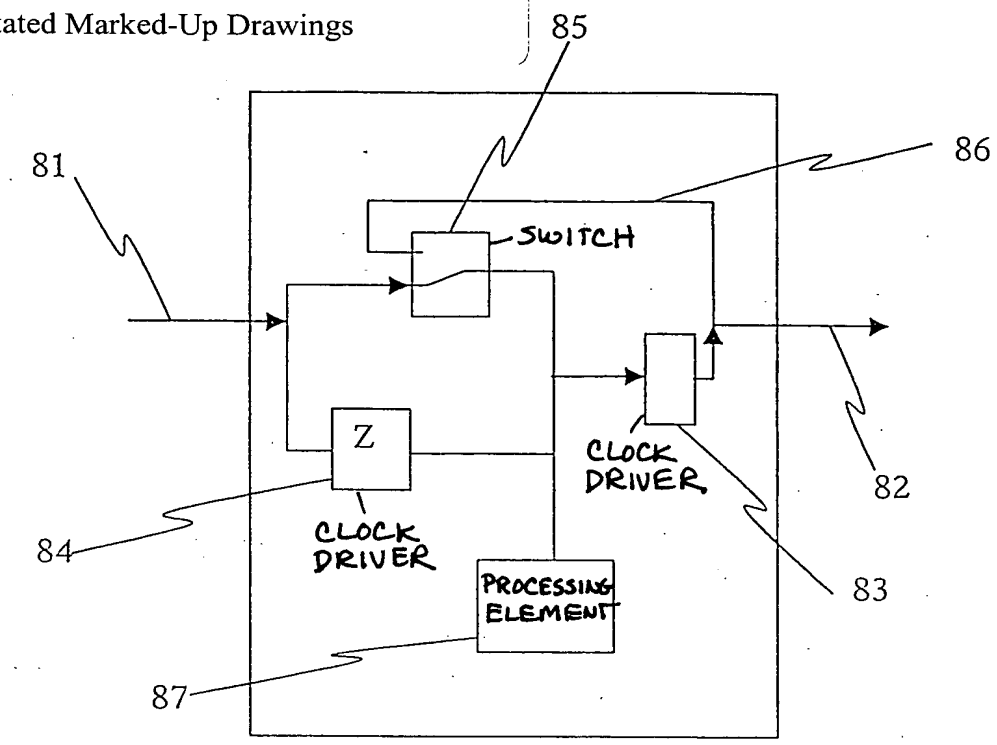
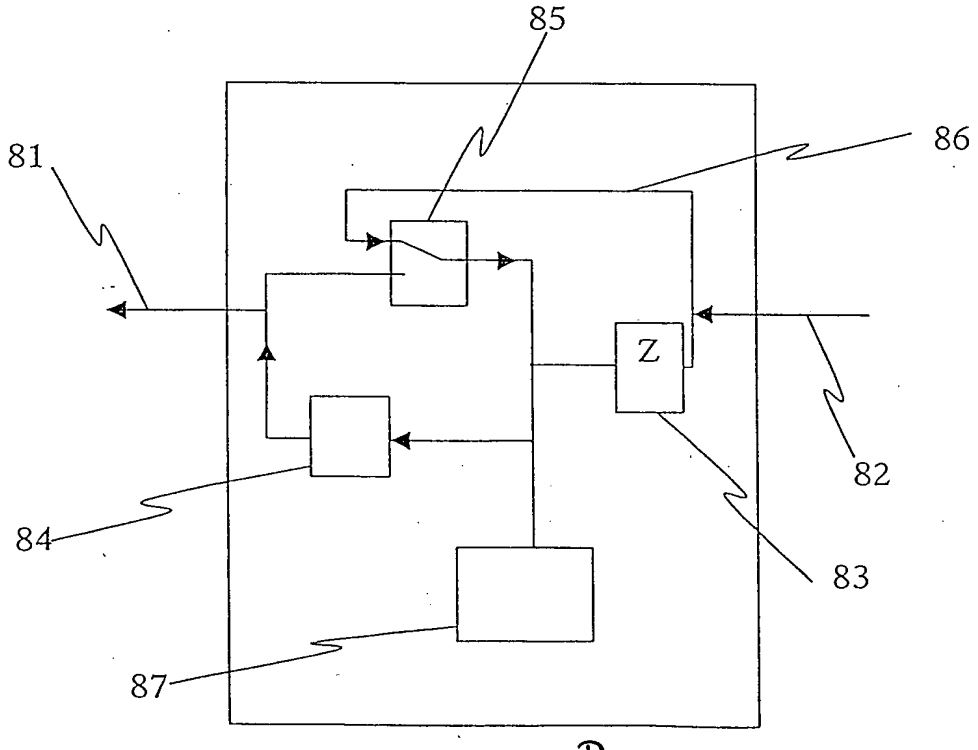
5
ARRAY
CLOCK GENERATOR
11b
9
4a
I/O PORT
ARRAY
13
1
2
3

Figure 7



A

Figure 8a



B

Figure 8b